Enabling a Reliable STT-MRAM Main Memory Simulation

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Motivation

DRAM is the dominant main memory technology for decades (mature technology).

Numerous studies forecasted end of DRAM:
- Scalability
- Resiliency
- Reliability
- Refresh/Power

Emerging technologies
- PCM
- NAND
- STT-MRAM
- RRAM
- 3D X-Point
STT-MRAM (Spin Transfer Torque Magnetic Random Access Memory)

Magnetic Tunneling Junction (MTJ)

Free magnetic layer

Fixed magnetic layer

STT-MRAM cell
Low resistance MTJ - Logical “0”

Free magnetic layer

Fixed magnetic layer

STT-MRAM cell
High resistance MTJ - Logical “1”

STT-MRAM Properties

- Non volatile
- Byte addressable
- High endurance
- High scalability
- CMOS compatible
Several studies analyze STT-MRAM as a cache memory:

- Clean replacement
- Integrate with SRAM
- EWT Scheme
- Trading-off non-volatility
- Retention time
STT-MRAM is rapidly catching up with DRAM capacity.
Only a few studies evaluate STT-MRAM as the Main Memory

- Questionable time parameters
- Unreliable source of timing
- Obsolete
- Preliminary study
STT-MRAM Main Memory Timing

STT-MRAM Timing Parameters Obstacles
- STT-MRAM Main Memory timing has not been Standardized
- Manufacturers won’t reveal timing information

Our approach to find reliable timing
- Patent applications & scientific papers
- DDRx compatibility
- Seamless Integration
STT-MRAM Cell Array

STT-MRAM vs DRAM cell array
### DRAM vs STT-MRAM timing

#### Timing parameters associated with row operation

<table>
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<tr>
<th>Parameter</th>
<th>DRAM</th>
<th>ST-1.2</th>
<th>ST-1.5</th>
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#### Timing parameters not associated with row operation

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<td>tXP</td>
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The numbers are bound to be changed with time. But methodology should persist.

*DDR3 1600 Cycles*
Simulation Infrastructure

SPEC CPU 2006 Benchmarks
- Video Compression
- Quantum Computing
- Programming Languages
- Artificial Intelligence
- Quantum Chemistry
- Molecular Dynamics
- Fluid Dynamics
- General Relativity

* Three sets of STT-MRAM timings were tested by varying key timing parameters (Sensitivity Analysis).

ZSim System Simulator
(Sandy bridge EP E5 2670)

DRAMSim2
(DDR3 DRAM 1600 STT-MRAM*)
Floating point benchmarks: speedup ranges from 0% (tonto) to 7.4% (milc); 2.7% on average.

Integer benchmarks: speedup ranges from 0.3% (gobmk) to 3.2% (hmmer); 1.4% on average.
Results – 1.5x Slower STT-MRAM

Floating point benchmarks: slowdown ranges from 0% (gamess) to 10.1% (lbm); 2.8% on average.

Integer benchmarks: slowdown ranges from -0.2% (h264ref) to 2.6% (sjeng); 1.1% on average.
Results – 2.0x Slower STT-MRAM

Floating point benchmarks: slowdown ranges from 0% (gamess) to 29.6% (lbm); 11.9% on average.

Integer benchmarks: slowdown ranges from 0.2% (h264ref) to 9.3% (bzip2); 5.1% on average.
Conclusions

- STT-MRAM is a promising memory technology
- Lack of reliable timing parameters of STT-MRAM
- First study to introduce detailed timing parameters
- Comparable performance w.r.t DRAM
- Enable researchers for reliable system level research
THANK YOU!