



# MEMSYS 2018

The International Symposium on Memory Systems

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*Mon Oct 1*      **Welcome Reception**      *5:00 – 9:00 pm*

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*Tue Oct 2*      **Breakfast**      *8:00 am*

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*8:50 am*      **Opening Remarks**

*9:00 am*      **Software Keynote: Brian Barrett**  
*Principal Engineer*  
*Amazon Web Services, Amazon.com*

*10:00 am*      **Break**

*10:20 am*      **Session 1: Datacenters and Large Memories**      *p.1*

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**Session Chair:** Matthias Jung, Fraunhofer IESE

*10:20 am*      Design Guidelines for High-Performance SCM Hierarchies      *p.3*  
*Dmitrii Ustiugov (EcoCloud, EPFL), Alexandros Daglis (EcoCloud, EPFL), Javier Picorel (Huawei), Mark Sutherland (EcoCloud, EPFL), Edouard Bugnion (EcoCloud, EPFL), Babak Falsafi (EcoCloud, EPFL), Dionisios Pneumatikatos (FORTH-ICS & ECE-TUC)*

*10:40 am*      A Comprehensive Memory Analysis of Data Intensive Workloads on Server Class Architecture      *p.19*  
*Hossein Mohammadi Makrani (George Mason University), Hossein Sayadi (George Mason University), Sai Manoj Pudukotai Dinakarra (George Mason University), Setareh Rafatirad (George Mason University), Houman Homayoun (George Mason University)*

*11:00 am*      HUB: Hupage Ballooning in Kernel-Based Virtual Machines      *p.31*  
*Jingyuan Hu (Peking University), Xiaokuang Bai (Peking University), Sai Sha (Peking University), Yingwei Luo (Peking University), Xiaolin Wang (Peking University), Zhenlin Wang (Michigan Technological University)*

**Rambus**

**arm**



**Micron**



**Sandia National Laboratories**



**Lawrence Livermore National Laboratory**

**NORTHROP GRUMMAN**

**SAMSUNG**

11:20 am	Memory Failure Prediction Using Online Learning <i>Xiaoming Du (Intel), Cong Li (Intel)</i>	p.38
11:40 am	Quantify the Performance Overheads of PMDK <i>William Wang (Arm Research), Stephan Diestelhorst (Arm Research)</i>	p.50
12:00 pm	<b>Conference Lunch</b>	
1:00 pm	<b>Session 2: Memory for Parallel Systems &amp; Architectures I</b>	p.53
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<b>Session Chair:</b> Scott Lloyd, Lawrence Livermore National Lab		
1:00 pm	A Load Balancing Technique for Memory Channels <i>Byoungchan Oh (University of Michigan), Nam Sung Kim (University of Illinois at Urbana-Champaign), Jeongseob Ahn (Ajou University), Bingchao Li (Civil Aviation University of China), Ronald Dreslinski (University of Michigan), Trevor Mudge (University of Michigan)</i>	p.55
1:20 pm	Cooperative NV-NUMA: Prolonging Non-Volatile Memory Lifetime through Bandwidth Sharing <i>Mohammad Reza Jokar (University of Chicago), Lunkai Zhang (University of Chicago), Frederic Chong (University of Chicago)</i>	p.67
1:40 pm	GraphIA: An In-situ Accelerator for Large-scale Graph Processing <i>Gushu Li (University of California, Santa Barbara), Guobao Dai (Tsinghua University), Shuangchen Li (University of California, Santa Barbara), Yu Wang (Tsinghua University), Yuan Xie (University of California, Santa Barbara)</i>	p.79
2:00 pm	Dynamic Fine-Grained Sparse Memory Accesses <i>Berkin Akin (Intel), Chiachen Chou (Google), Jongsoo Park (Facebook), Christopher Hughes (Intel), Rajat Agarwal (Intel)</i>	p.85
2:20 pm	Memory-System Design Challenges in Realizing Monolithic Computers <i>Meenatchi Jagasivamani (University of Maryland), Candace Walden (University of Maryland), Devesh Singh (University of Maryland), Luyi Kang (University of Maryland), Shang Li (University of Maryland), Mehdi Asnaashari (Crossbar Inc.), Sylvain Dubois (Crossbar Inc.), Bruce Jacob (University of Maryland), Donald Yeung (University of Maryland)</i>	p.98
2:40 pm	<b>Break</b>	
3:00 pm	<b>Session 3: DRAM Issues and Architectures</b>	p.105
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<b>Session Chair:</b> Robert Voigt, Northrop Grumman		
3:00 pm	Main Memory Latency Simulation: The Missing Link <i>Rommel Sanchez Verdejo (Barcelona Supercomputing Center), Kazi Asifuzzaman (Barcelona Supercomputing Center), Milan Radulovic (Barcelona Supercomputing Center), Petar Radojkovic (Barcelona Supercomputing Center), Eduard Ayguade (Barcelona Supercomputing Center), Bruce Jacob (University of Maryland)</i>	p.107
3:20 pm	Cocoa: Synergistic Cache Compression and Error Correction in Capacity Sensitive Last Level Caches <i>Chao Yan (Northwestern University), Russ Joseph (Northwestern University)</i>	p.117

3:40 pm	Opportunistic Compression for Direct-Mapped DRAM Caches <i>Alaa Alameldeen (Intel), Rajat Agarwal (Intel)</i>	p.129
4:00 pm	Tackling Memory Access Latency Through DRAM Row Management <i>Sriveshan Srikanth (Georgia Institute of Technology), Lavanya Subramanian (Intel Labs), Sreenivas Subramoney (Intel Labs), Thomas Conte (Georgia Institute of Technology), Hong Wang (Intel Labs)</i>	p.137
4:20 pm	Efficient Coding Scheme for DDR4 Memory Subsystems <i>Kira Kraft (Technische Universität Kaiserslautern), Deepak M. Mathew (Technische Universität Kaiserslautern), Chirag Sudarshan (Technische Universität Kaiserslautern), Matthias Jung (Fraunhofer), Christian Weis (Technische Universität Kaiserslautern), Norbert Wehn (Technische Universität Kaiserslautern), Florian Longnos (Huawei Technologies Co. Ltd, Data Center Technologies Lab)</i>	p.148
4:40 pm	<b>Break</b>	
5:00 – 7:00 pm	<b>Spirited Discussion</b>	
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	Memory Systems Problems and Solutions	
	<ul style="list-style-type: none"> <li>• Keren Bergman, Columbia University</li> <li>• Phil Emma, Systems Technology &amp; Architecture Consulting</li> <li>• Adolfo Hoisie, Brookhaven National Lab</li> <li>• Rob Ross, Argonne National Lab</li> <li>• Jeffrey Vetter, Georgia Tech &amp; Oak Ridge National Lab</li> <li>• Ke Zhang, Institute of Computing Technology, Chinese Academy of Sciences</li> </ul>	
7:30 pm	<b>Dinner</b> — <i>Regular attendees on your own</i> <i>Program Committee dinner meeting — McCormick &amp; Schmick's Harborside</i>	

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Wed Oct 3	<b>Breakfast</b>	8:00 am
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9:00 am	<b>Hardware Keynote:</b> <i>Steve Wallach</i> <i>Founder of Convey, purchased by Micron, now Director of Design-Engineering</i> <i>Micron</i>	
10:00 am	<b>Break</b>	
10:20 am	<b>Session 4: Memory for Parallel Systems &amp; Architectures II</b>	p.159
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	<b>Session Chair:</b> Kurt Keville, MIT	
10:20 am	Linking Parallel Algorithmic Thinking to Many-Core Memory Systems and Speedups for Boosted Decision Trees <i>James Edwards (University of Maryland), Uzi Vishkin (University of Maryland)</i>	p.161
10:40 am	Profile-Guided Scope-Based Data Allocation Method <i>Hugo Brunie (CEA/DAM Ile de France), Julien Jaeger (CEA/DAM Ile de France), Patrick Carribault (CEA/DAM Ile de France), Denis Barthou (Bordeaux INP)</i>	p.169

11:00 am	Enhancing High-Level Synthesis of Accelerators for Memory-bound Workloads <i>Marco Minutoli (Pacific Northwest National Laboratory), Vito Giovanni Castellana (Pacific Northwest National Laboratory), Antonino Tumeo (Pacific Northwest National Laboratory), Nicola Saporetti (Politecnico di Milano), Stefano Devecchi (Politecnico di Milano), Marco Lattuada (Politecnico di Milano), Pietro Fezzardi (Politecnico di Milano), Fabrizio Ferrandi (Politecnico di Milano)</i>	p.183
11:20 am	Achieving Transparency Mapping Parallel Applications: A Memory Hierarchy Affair <i>Edgar A Leon (Lawrence Livermore National Laboratory), Matthieu Hautreux (French Alternative Energies and Atomic Energy Commission)</i>	p.187
11:40 am	Hardware Transactional Persistent Memory <i>Ellis Giles (Rice University), Kshitij Doshi (Intel), Peter Varman (Rice University)</i>	p.192
12:00 pm	<b>Conference Awards Luncheon</b>	
1:00 pm	<b>Session 5: Modeling and Simulation</b>	p.209
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	<b>Session Chair:</b> Ishwar Bhati, Intel	
1:00 pm	HMCTherm: A Cycle-accurate HMC Simulator Integrated with Detailed Power and Thermal Simulation <i>Zhiyuan Yang (University of Maryland), Michael Zuzak (University of Maryland), Ankur Srivastava (University of Maryland)</i>	p.211
1:20 pm	Design Space Exploration of Near Memory Accelerators <i>Scott Lloyd (Lawrence Livermore National Laboratory), Maya Gokhale (Lawrence Livermore National Laboratory)</i>	p.220
1:40 pm	Fine-Grained Data Usage Analysis by Access Sampling: Seeing the Data That Is Not There <i>Zhibzhou Zhang (University of California, Santa Barbara), Chencheng Ye (Huazhong University of Science and Technology), Rahman Lavaee (Google), Ning Gu (Rutgers University), Chen Ding (University of Rochester)</i>	p.223
2:00 pm	Footprint Modeling of Cache Associativity and Granularity <i>Hao Luo (Google), Guoyang Chen (Alibaba Group), Fangzhou Liu (University of Rochester), Pengcheng Li (Google), Chen Ding (University of Rochester), Xipeng Shen (North Carolina State University)</i>	p.234
2:20 pm	Data-Driven Spatial Locality <i>Svetozar Miucin (University of British Columbia), Alexandra Fedorova (University of British Columbia)</i>	p.245
2:40 pm	<b>Break</b>	
3:00 pm	<b>Session 6: Exotic Technologies and Applications</b>	p.257
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	<b>Session Chair:</b> Petar Radojkovic, Barcelona Supercomputing Center	
3:00 pm	Optically Connected and Reconfigurable GPU Architecture for Optimized Peer-to-Peer Access <i>Erik Anderson (Columbia University), Jorge Gonzalez (University of Campinas), Alexander Gazman (Columbia University), Rodolfo Azevedo (University of Campinas), Keren Bergman (Columbia University)</i>	p.259

3:20 pm	Multi-Level Memristive Voltage Divider: Programming Scheme Trade-offs <i>Tobias Lieske (Friedrich-Alexander-University), Mehrdad Biglari (Friedrich-Alexander University), Dietmar Fey (University Erlangen-Nuremberg)</i>	p.261
3:40 pm	AWGR-based Optical Processor-to-Memory Communication for Low-latency, Low-energy Vault Accesses <i>Sebastian Werner (University of California, Davis), Pouya Fotoubi (University of California, Davis), Roberto Proietti (University of California, Davis), S.J. Ben Yoo (University of California, Davis)</i>	p.271
4:00 pm	Leveraging MLC STT-RAM for Energy-efficient CNN Training <i>Hengyu Zhao (University of California San Diego), Jisben Zhao (University of California San Diego)</i>	p.281
4:20 pm	Memory-System Requirements for Convolutional Neural Networks <i>Antara Ganguly (Indian Institute of Technology Bombay), Virendra Singh (Indian Institute of Technology Bombay), Rajeev Muralidhar (Intel), Masahiro Fujita (University of Tokyo)</i>	p.293

4:40 pm **Break**

5:00 – 7:00 pm **Spirited Discussion**

New and Cool Memory Technologies

- Shekhar Borkar, Qualcomm
- Ron Brightwell, Sandia National Labs
- Wendy Elsasser, Arm
- Michael Healy, IBM
- David Resnick, “in the process of retiring ...”
- Owens Walker, United States Naval Academy

7:30 pm **Conference Dinner & Entertainment** — Bobby McKeys

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*Thu Oct 4* **Breakfast** 8:00 am

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8:40 am **Session 7: Invited Papers** p.301

**Session Chair:** David Donofrio, Berkeley Lab

8:40 am	PPT-GPU: Performance Prediction Toolkit for GPUs (Identifying the impact of caches: Extended Abstract) <i>Yehia Arafa (New Mexico State University), Abdel-Hameed Badawy (New Mexico State University), Gopinath Chennupati (Los Alamos National Laboratory), Nandakishore Santhi (Los Alamos National Laboratory), Stephan Eidenbenz (Los Alamos National Laboratory)</i>	p.303
9:00 am	Open2C: Open-source Generator for Coherent Cache Memory Subsystem Exploration <i>Anastasiia Butko (Lawrence Berkeley National Lab), Albert Chen (University of California, Berkeley), David Donofrio (Lawrence Berkeley National Lab), Farzad Fatollahi-Fard (Lawrence Berkeley National Lab), John Shalf (Lawrence Berkeley National Lab)</i>	p.305
9:20 am	Demonstration of Superconducting Memory for an RQL CPU <i>Randall Burnett (Northrop Grumman Corporation), Ryan Clarke (Northrop Grumman Corporation), Tim Lee (Northrop Grumman Corporation), Harold Hearne (Northrop Grumman Corporation), Jacob</i>	p.312

*Vogel (Northrop Grumman Corporation), Quentin Herr (Northrop Grumman Corporation), Anna Herr (Northrop Grumman Corporation)*

9:40 am	Towards Detection of Modified Firmware on Solid State Drives via Side Channel Analysis	<i>insert</i>
	<i>Dane Brown (U.S. Naval Academy), Owens Walker (U.S. Naval Academy), Ryan Rakvic (U.S. Naval Academy), Robert Ives (U.S. Naval Academy), Hau Ngo (U.S. Naval Academy), James Shbey (U.S. Naval Academy), Justin Blanco (U.S. Naval Academy)</i>	
10:00 am	<b>Break</b>	
10:20 am	<b>Session 8: Experimentations &amp; Optimizations</b>	<i>p.315</i>
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	<b>Session Chair:</b> Zeshan Chishti, Intel	
10:20 am	Architecting a Hardware-Managed Hybrid DIMM Optimized for Cost/Performance	<i>p.317</i>
	<i>Fred Ware (Rambus Inc.), Javier Bueno (Metempsy), Liji Gopalakrishnan (Rambus Inc.), Brent Haukness (Rambus Inc.), Chris Haywood (Rambus Inc.), Toni Juan (Metempsy), Eric Linstadt (Rambus Inc.), Sally A. McKee (Clemson University), Steven C. Woo (Rambus Inc.), Kenneth L. Wright (Rambus Inc.), Craig Hampel (Rambus Inc.), Gary Bronner (Rambus Inc.)</i>	
10:40 am	A Performance & Power Comparison of Modern High-Speed DRAM Architectures	<i>p.331</i>
	<i>Shang Li (University of Maryland), Dhiraj Reddy (University of Maryland), Bruce Jacob (University of Maryland)</i>	
11:00 am	A Raspberry Pi Operating System for Exploring Advanced Memory System Concepts	<i>p.344</i>
	<i>Pascal Francis-Mezger (University of Maine), Vincent Weaver (University of Maine)</i>	
11:20 am	Stake: A Coupled Simulation Environment for RISC-V Memory Experiments	<i>p.355</i>
	<i>John Leidel (Tactical Computing Laboratories)</i>	
11:40 am	Driving into the Memory Wall: The Role of Memory for Advanced Driver Assistance Systems and Autonomous Driving	<i>p.367</i>
	<i>Matthias Jung (Fraunhofer), Sally A. McKee (Clemson University), Chirag Sudarshan (Technische Universität Kaiserslautern), Christoph Drogmann (Fraunhofer), Christian Weis (Technische Universität Kaiserslautern), Norbert Wehn (Technische Universität Kaiserslautern)</i>	
12:00 pm	<b>Postamble:</b> J. Thomas Pawłowski Chief Technologist / Micron Fellow Architecture Development, Micron	
12:40 pm	<b>Closing Remarks</b>	